DECLARATION

I, Setsuko Nakata, residing at 12-16, Sakuragaoka 1-chome, Kugenuma, Fujisawa-shi, Kanagawa 251-0027, Japan, do solemnly and sincerely declare that I well understand both Japanese and English languages and the attached English version is a full, true and faithful translation of Japanese Patent Application Number 2000/372231 filed on December 7, 2000 in the name of FUJITSU LIMITED.

And I made this solemn declaration conscientiously believing the same to be true.

This 19th day of March ,

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[Name of Document] SPECIFICATION

[Title of the Invention] TESTING APPARATUS AND TESTING METHOD FOR AN INTEGRATED CIRCUIT

[Scope of Claim]

[Claim 1] A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate test patterns;

a pattern modifier for modifying said generated test patterns according to external inputs; and

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit;

the test patterns modified by said pattern modifier being inputted to said plural shift registers.

[Claim 2] A testing apparatus for an integrated circuit comprising:

a plurality of shift registers, to which test patterns are inputted, configured with sequential circuit elements inside said integrated circuit;

a mask for making an indeterminate state in outputs from said plural shift registers and converting the indeterminate state to a specified state; and

an output verifier for verifying output results masked by said mask.

[Claim 3] A testing apparatus for an integrated circuit comprising:

a pattern generator built in said integrated circuit to generate test patterns;

a pattern modifier for modifying the test patterns generated by said pattern generator according to external inputs;

a plurality of shift registers configured with sequential circuit elements inside said integrated circuit;

a mask for masking an indeterminate state in outputs from said plural shift registers, to which the test pattern modified by said pattern modifier are inputted, to convert the indeterminate state to a specified state; and

an output verifier for verifying output results masked by said mask.

[Claim 4] The testing apparatus according to claim 2 or 3, wherein said output verifier includes a means for compressing the masked output results.

[Claim 5] A testing method for an integrated circuit comprising the steps of:

generating test patterns by a pattern generator built in said integrated circuit;

modifying said generated test patterns according to external inputs; and

inputting said modified test patterns to a plurality of shift registers configured with sequential circuit elements inside said integrated circuit.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates to a testing apparatus and a testing method for detecting manufacturing failure of an integrated circuit.

[0002]

[Prior Art]

Detection of manufacturing failure of an integrated circuit (LSI) is performed by applying an appropriate signal value to an input pint of the LSI using a tester, and comparing a signal value appearing at an output pin with an expected result. The signal value applied to the input pin and the expected value that should appear at the output pin are collectively called a test pattern, in general.

[0003]

Defect occurring in an LSI due to manufacturing failure of the LSI is called fault. In order to verify all faults that may occur inside the LSI, a lot of test patterns are necessary. A ratio of the number of faults that can be verified with a certain pattern to the number of all faults estimated inside the LSI is called a detection ratio (or fault coverage), used as a scale when the quality of the test pattern is considered.

[0004]

When the LSI contains a sequential circuit element [flip-flop (F/F), latch, or RAM], complexity of

creation of the test pattern remarkably increases. For this, performed is scan design, where a shift register (called a Scan Path) is configured with sequential circuit elements (mainly F/Fs) inside the LSI, a desired value is shifted-in the shift registers at the time of test, and a value of the shift register is read out after a clock is applied.

[0005]

In such a circuit, Deterministic Stored Pattern Test (DSPT) is widely employed. DSPT is performed by storing test patterns created by Automatic Test Pattern Generator (ATPG) in a tester (ATE: Automatic Test Equipment).

[0006]

FIG. 8 is a diagram for illustrating a known scan design. In FIG. 8, concept of the scan design is shown as a block diagram. As shown in this block diagram, a plurality of scan paths (shift registers) #0, #1, …, and #n-1 that are routes for testing an LSI are formed with a plurality of F/Fs that are storage elements. A test pattern is shifted-in from the left end of the scan paths #0, #1, … and #n-1, and a result of the test is outputted from the right end of the same. With the recent progress in integration of LSIs, the number of sequential circuit elements contained inside is increased. For this, the following problems arise when DPST, which repetitively performs setting and reading on all sequential circuit

elements configuring the scan paths, is applied.

[0007]

1. Increase in testing time

2. Shortage of memory capacity of tester due to increasing test data

In order to solve these problems, Built In Self Test (BIST) is performed. In BIST, a pattern generated by a pseudo random pattern generator is applied to an internal circuit of an LSI, and an outputted result from the internal circuit is verified and stored by an output verifier. As the pseudo random pattern generator and the output verifier, there is used a linear feedback shift register (LFSR) in many cases. Particularly, the output verifier is called a multiple input signature register (MISR) since it compresses and stores outputted results as signature.

[0008]

FIG. 9 is a diagram for illustrating a known BIST circuit. In FIG. 9, a concept of the BIST circuit is shown as a block diagram. As shown in this block diagram, a linear feedback shift register (LFSR) 2, a phase shifter 3, scan paths #0, #1, …, and #n-1, a space compactor 6 and a multi-input signature register (MISR) 7 are built in the BIST circuit.

[0009]

A pseudo random pattern generated by the LFSR 2 is inputted to the leading F/F of each of the scan paths #0, #1, …, and #n-1 through the phase shifter 3. Outputted

results from the scan paths #0, #1, …, and #n-1 are compressed into about the number of bits (for example, 32 bits) of the MISR 7 by the space compactor 6, then the results are further compressed and stored by the MISR 7.

[0010]

Since a pattern generator is mounted inside the LSI in BIST, an enormous number of test patterns can be generated within a short time. Since the MISR 7 compresses and stores results of the test, the amount of data to be loaded in the tester can be greatly decreased.

[0011]

[Problems to be Solved by the Invention]

In the test on LSIs, DSPT based on the scan design and BIST where a test circuit is built in are used now.

[0012]

DSPT enables a test of a very high quality (detection ratio) since it uses test patterns created by an ATPG, and can readily add test patterns. However, the number of test patterns is largely increased for a large scale LSI, it thus becomes difficult to store all test patterns created by the ATPG on the memory of a tester, and the testing time by the tester is increased. Therefore, a very expensive tester is required to carry out DSPT.

[0013]

BIST can solve the problems of the above DSPT, but has some problems. Since pseudo random patterns are used in BIST, the quality of the test is in question. In

order to increase the fault coverage, it is necessary to apply DSPT as an additional test, or insert such a test point in the internal circuit as to increase controllability and observability. MISR is used to compress data in BIST. However, even once an indeterminate state is captured, all registers in the MISR are brought into the indeterminate state because of the structural nature of the MISR, which makes the test impossible.

[0014]

Since sequential circuit elements including a RAM inside an LSI are generally in the indeterminate state when the power source is turned on, it is necessary to beforehand apply a pattern to initialize these sequential circuit elements, or to invent the circuit such as to prevent the indeterminate state from propagating to the MISR. Other than this, the designer is forced server limitations in design when the BIST is applied to an actual circuit in order to prevent a conflict or a float state caused by the random pattern from occurring when a bus and the like is designed, for example. Additionally, inserting the BIST circuit and a test point causes area overhead of the circuit.

[0015]

In the light of the above problems, an object of the present invention is to overcome problems of the DSPT and BIST, and to execute a high quality test within a short time. The present invention is to provide a method without

forcing server design limitations on the designer at this time, which can dispense with an expensive tester.

[0016]

[Means for Solving the Problems]

FIG. 1 is a diagram for illustrating a principle of this invention. In FIG. 1, reference character 2a denotes a pattern generator, 4 a pattern modifier, 5 a mask , 7a an output verifier, and #0 to #n-1 shift registers (scan paths).

[0017]

To solve the above problems, the present invention has the following means.

[0018]

(1) A pattern generator 2a built in the integrated circuit to generate test patterns, a pattern modifier 4 for modifying the generated test patterns according to external inputs, and a plurality of shift registers #0 to #n-1 configured with sequential circuit elements inside the integrated circuit. The test patterns modified by the pattern modifier 4 are inputted to the shift registers #0 to #n-1. Whereby, the number of scan paths that are the shift registers #0 to #n-1 is increased to decrease the number of stages of the scan paths, which allows a testing time for the integrated circuit (LSI) to be shortened. At this time, only significant data (information on F/Fs which require setting) is supplied form a tester (external input) and modified, so that the

quantity of data to be stored in the tester can be decreased.

[0019]

(2) A testing apparatus according to this invention comprises a plurality of shift registers #0 to #n-1, to which test patterns are inputted, configured with sequential circuit elements inside the integrated circuit, a mask 5 masking the indeterminate state in outputs from the above shift registers #0 to #n-1 and converting the indeterminate state to a specified state, and an output verifier 7a verifying the masked output results. Even when results of the sequential circuit elements (internal F/Fs) are compressed and read out to the outside, a result of the compression is not spoiled by the indeterminate state (X state).

[0020]

(3) A testing apparatus according to this invention comprises a pattern generator 2 built in an integrated circuit to generate test patterns, a pattern modifier 4 modifying the generated test patterns according to external inputs, a plurality of shift registers #0 to #n-1 configured with sequential circuit elements inside the integrated circuit, a mask 5 masking the indeterminate state in outputs from the plural shift registers #0 to #n-1, to which the test patterns modified by the pattern modifier 4 are inputted, and converting the indeterminate state to a specified state, and an output verifier 7a verifying the masked output results. Whereby, it becomes possible to

increase the number of the scan paths, which permits a shorter time period of the test on the integrated circuit (LSI). It becomes also possible to decrease the amount of data to be stored in the tester because only meaningful data is supplied from the tester (external input) and modified, and to avoid a result of the compression from being spoiled by the indeterminate state.

[0021]

(4) The testing apparatus for an integrated circuit described in the above (2) or (3), the output verifier 7a may include a means for compressing the masked output results, whereby results of the internal F/Fs can be efficiently stored in the output verifier 7a.

[0022]

[Embodiment of the Invention]

When a higher quality test is made on an integrated circuit (LSI), a problem arises that a method using a pseudo random pattern has a limitation like BIST in which a test circuit is built in. Namely, since a fault that is difficult to be found by the random pattern exists, it is necessary to insert a test point to improve controllability and observability of the circuit, and generate a great number of random patterns. Nevertheless, it is impossible to realize the same quality as the deterministic pattern generated by the ATPG.

[0023]

On the other hand, when a pattern is generated

by the ATPG, a fault at one point in the internal circuit is basically supposed, and a pattern for detecting it is created. Such pattern will be referred as an ATPG pattern. The ATPG pattern is configured with set values of all internal F/Fs, and state values of all F/Fs obtained after a system clock is applied. The number of sequential circuit elements (F/Fs) that are required to set in order to detect this fault with a generated pattern is much smaller than the number of all F/Fs.

[0024]

FIG. 2 is a diagram for illustrating a state of distribution of the number of set F/Fs of the ATPG. In FIG. 2, the horizontal axis represents the number of ATPG patterns for detecting faults of the internal circuit, while the vertical axis represents the number of F/Fs to which values for detecting the faults should be set. Basically, the ATPG creates one pattern to detect one fault at a time. Accordingly, the ATPG pattern is created with the set F/Fs being sparse. For this, it is a main stream that patterns are such compressed as to detect a plurality of faults with one ATPG pattern (which avoids double setting, in this case). Data shown in FIG. 2 is a result of compaction of patterns. An ATPG pattern in which the number of set F/Fs is more than a thousand is such created and set as to detect a plurality of faults. Incidentally, the ATPG patterns are sorted in the descending order of the set F/Fs.

[0025]

In DSPT, it is generally necessary to supply data of (the number of ATPG patterns) × (the number of all F/Fs) from a tester to a test target LSI. This corresponds to data in an entire area (21281×2755) of the rectangle shown in FIG. 2. On the other hand, the amount of significant data set by the ATPG is only a shadowed area in the lower part in FIG. 2. For instance, in the first ATPG pattern, it is necessary to set data to 1272 F/Fs, while in the thousandth ATPG pattern, it is necessary to set data to about 50 F/Fs. As this, the number of sequential circuit elements (F/Fs) that the ATPG needs to set values is extremely small as compared with the number of all the F/Fs (21281).

[0026]

According to this invention, only significant data set by the ATPG can be supplied from the tester, and a deterministic pattern can be applied to a test target LSI.

[0027]

In the case of an LSI applied scan design, one ATPG pattern is divided into a plurality of shift patterns for scan paths, and applied from the tester to the LSI, and F/Fs inside the LSI are distributed to a plurality of the scan paths which can be shifted in parallel. Whereby, the testing time can be shortened. At this time, the testing time in the LSI applied scan design is:

(the number of ATPG patterns) × (the number of stages of scan path) × (test cycle).

In this case, the number of stages of the scan path in the above formula is the number of F/Fs in a scan path to which a largest number of F/Fs are distributed. The test cycle is a clock cycle supplied to the LSI by the tester, which depends on the performance of the tester.

[0028]

Since it is possible to operate the internal pattern generator in BIST, the testing time can be shortened by shortening the clock cycle (by shortening the test cycle). Further, it is possible to readily increase the number of scan paths by increasing the number of output pins of the pattern generator. As a result, it is possible to decrease the number of stages of the scan path, thereby shortening the testing time.

[0029]

In DSPT, it is necessary to set an input pin and an output pin to each scan path, and connect them to a tester. Since the number of these input and output pins depends on the performance of the tester, the number of scan paths cannot be increased more than limitations of the tester.

[0030]

According to this invention, the number of the scan paths is increased to decrease the number of stages of the scan path like BIST, thereby shortening the testing time of an LSI. At this time, data given from the tester is invented (for example, chain information being compressed by a decoder circuit or the like), and only

significant or meaningful data (information on F/Fs which requires the setting) is supplied from the tester using a small number of pins within the limitations of the tester.

[0031]

Although the number of F/Fs to which values should be set by the ATPG is small, a random pattern is set to the remaining F/Fs when the pattern is actually supplied from the tester. Reason of this is that it is expected that a fault other than the relevant fault is incidentally verified with the pattern. According to this invention, a circuit similar to BIST is used to supply a random pattern to most of the F/Fs other than the F/Fs to which setting information is supplied from the tester for the above purpose, as well.

[0032]

In the LSI test, it is necessary that values are set to the internal F/Fs through a scan path from the tester, a clock of the system is applied, after that, the value of each of the internal F/Fs is read out through the scan path and compared with an expected value. When the internal F/Fs are required to operate at a high speed or the number of scan paths is large, BIST employs a method of compressing results of the internal F/Fs and storing them, and reading out them to the outside by the tester and comparing them with expected values, afterwards, not hastily. For this purpose, there is used an MISR configured with an LFSR and an EOR (exclusive OR) gate.

[0033]

According to this invention, it is necessary to compress results of the internal F/Fs and read them out like BIST in order to increase the number of the scan paths. At this time, the indeterminate state (X state) of a RAM or the like might spoil a result of the compression in the MISR as pointed out in the description of the problem of BIST. An EOR gate is used at an entrance of the MISR, and an EOR gate is also used in a feedback loop of the MISR. If the indeterminate state is present in even one input to the EOR gate, an output of the EOR gate is brought into the indeterminate state. For this, all registers in the MISR in which an EOR gate is interposed in the feedback loop thereof are degenerated into the indeterminate state. According to this invention, the indeterminate state is masked on the output's side of the scan path.

[0034]

FIG. 3 is a diagram illustrating a testing apparatus according to an embodiment of this invention. In FIG. 3, the testing apparatus comprises a linear feedback shift register (LFSR) 2, a phase shifter 3, a pattern modifier (Pattern Modifying Part) 4, scan paths #0, #1, …, and #n-1, a mask 5, a space compactor 6, and a multiple input signature register (MISR) 7.

[0035]

Pseudo random pattern generated by the LFSR 2 are inputted to the pattern modifier 4 through the phase shifter

3. Control signals from a tester are inputted to the pattern modifier 4 through control input pins or the like. The pattern modifier 4 modifies only a value for an F/F required to be set a value according to the control signals, and inputs and sets the value to the leading F/F of each of the scan paths #0, #1, …, and #n-1. The mask 5 masks the indeterminate value (X state) of the last F/F on the scan path #0, #1, …, or #n-1 according to the control signal inputted through the control input pin or the like, and inputs it to the space compactor 6. The space compactor 6 compresses values of the last F/Fs into about the number of bits (for example, 32 bits) of the MISR 7, and inputs them to the MISR 7. The MISR 7 further compresses data from the space compactor 6, and stores it.

[0036]

FIG. 4 is a diagram for illustrating a pattern generating part. In FIG. 4, it is assumed that the LFSR 2 as being the pattern generator has 128 scan paths. The pattern generating part is configured with the LFSR 2 and the phase shifter 3, wherein the LFSR 2 generates pseudo random patterns and inputs 128 random bit sequences to the pattern modifier 4 through the phase shifter 3. Other than this, the control signals are inputted to the pattern modifier 4 from the tester through the eight control input pins (a1 to a8). The 128 scan paths #0, #1, …, and #127 are connected to the pattern modifier 4. An output of the leading F/F of each of the 128 scan paths is fed back. The

pattern modifier 4 also controls a shift clock to the LFSR 2 (and the MISR 7) and a shift clock to the F/F on each of the scan paths #0, #1, …, and #127, thus can separately apply a shift clock to the leading F/F of each of the scan paths #0, #1, …, and #127.

[0037]

The pattern modifier 4 has a decoder circuit 21 to which lower seven bits (a2 to a8) of the control input are inputted. A signal value inputted to a specific one of the 128 scan paths #0, #1, …, and #127 is inverted by an EOR circuit 22. A code given to the control input and the operation of a corresponding code are described in detail below.

[0033]

(code)	(operation)
00000000	random pattern shift
00000001	invert the leading F/F on the scan path #1
00000010	invert the leading F/F on the scan path #2
.	
.	
01111111	invert the leading F/F on the scan path #127
10000000	random pattern shift to invert only the scan path #0
10000001	random pattern shift to invert only the scan path #1
10000010	random pattern shift to invert only the scan path #2

11111111 random pattern shift to invert only the scan path #127

When all bits of the control input is "0," a shift clock (negative clock) is supplied to the LFSR 2 and all the F/Fs on the scan paths through the input pins a10, and the random bit sequences created at the preceding clock by the LFSR 2 are shifted-in to the scan paths as they are.

[0039]

Namely, since the lower seven bits (a2 to a8) of the control input are "0," an output of an NOR circuit 24 is "1." Since the most significant bit (a1) of the control input is "0," an output of an NOR circuit 25 is "0." For this, multiplexers 23 transmit signals from the phase shifter 3 to the EOR (exclusive OR) circuits 22. The shift clock from the input pin a10 is directly supplied to the leading F/Fs on the scan paths, and is supplied to the LFSR 2 and the F/Fs excepting the leading F/F on the scan paths through an OR (logical sum) circuit 26. Incidentally, an AND circuit 27 is to prevent inversion of an input from the LFSR 2 to the scan path #0 when all bits of the control input is "0."

[0040]

When the control input is "1000000" to "1111111," the shift clock is supplied to the LFSR 2 and all the F/Fs on the scan paths, and random bit sequences created by the

LFSR 2 at the preceding clock are shifted-in to the scan paths. At this time, only a value of one scan path designated by the lower seven bits (a2 to 28) of the control input is inverted by the EOR circuit 22.

[0041]

Namely, since any one of the lower seven bits (a2 to a8) of the control input is "1," an output of the NOR circuit 24 is "0." Since the most significant bit (a1) of the control input is "1," an output of the NOR circuit 25 is "0." For this, the multiplexer 23 transmits signals from the phase shifter 3 to the EOR circuits 22. The shift clock from the input pin a10 is directly supplied to the leading F/Fs of the scan paths, and is supplied to the LFSR 2 and F/Fs excepting the leading F/Fs on the scan paths through the OR circuit 26. At this time, "1" is inputted to the EOR circuit 22 for one scan path designated by the lower seven bits of the control input from the decoder circuit 21. For this, a signal from the multiplexer 23 is inverted by the EOR circuit 22, then outputted to the leading F/F of the relevant scan path.

[0042]

When the control input is "00000001" to "01111111," the shift clock is supplied to only the leading F/F of a scan path, whereby not an output from the LFSR 2 but outputs from the leading F/Fs become effective and fed back to the leading F/Fs. At this time, only a value of one scan path designated by the lower seven bits of the

control input is inverted by the EOR circuit 22. By this operation, only a value of the leading F/F of the scan path designated by the lower seven bits of the control input is inverted.

[0043]

Namely, since any one of the lower seven bits (a2 to a8) of the control input is "1," an output of the NOR circuit 24 is "0." Since the most significant bit "a1" of the control input is "0," an output of the NOR circuit 25 is "1." For this, the shift clock through the input pin a10 is supplied to the leading F/Fs of the scan paths. However, the shift clock is not supplied to the LFSR 2 and F/Fs excepting the leading F/Fs on the scan path since an output of the OR circuit 26 becomes "1" due to an output of the NOR circuit 25. The multiplexer 23 transmits output signals from the leading F/Fs to the EOR circuits 22 according to the output "1" from the NOR circuit 25. At this time, "1" is inputted from the decoder circuit 21 to the EOR circuit 22 for one scan path designated by the lower seven bits of the control input, so that the signal from the multiplexer 23 is inverted by the EOR circuit 22, then outputted to the leading F/F of the designated scan path.

[0044]

FIG. 5 is a diagram for illustrating setting of random numbers (pseudo random patterns) and the ATPG. In a table of random numbers in FIG. 5, there are shown random numbers to be set to the F/Fs generated by the LFSR 2. In

the table of ATPG in FIG. 5, "-" corresponds to an F/F to which a value does not need to be set, whereas "1" and "0" are values to be set to F/Fs by the ATPG. Since the ATPG can grasp random numbers generated by the LFSR 2 by simulating the operation of the LFSR 2, the ATPG can find a value that needs to be modified in the table of random numbers. In FIG. 5, values surrounded by broken lines in the table of the ATPG differ from values in the table of random numbers. Accordingly, only the differing parts are modified.

[0045]

Concrete examples of input patterns for setting arbitrary values to the internal F/Fs using the circuit described above are shown below.

(pattern number)	(code)	(operation)
1	00000000	random pattern shift
2	10000011	random pattern shift to invert only the scan path #3
3	00000000	random pattern shift
4	10000001	random pattern shift to invert only the scan path #1
5	00000100	invert the leading F/F on the scan path #4
6	01111111	invert the leading F/F on the scan path #127
7	00000000	random pattern shift

In the examples shown above, seven patterns are supplied from the tester. In the first pattern (pattern number 1) where all the bits are "0," a random pattern shifting operation is carried out. In the second pattern, a random pattern shifting operation of inverting only an input value to the scan path #3 ("0" being inverted to "1") is carried out. In the third pattern where all the bits are "0," the random pattern shifting operation is carried out. In the fourth pattern to the sixth pattern, one stage of the scan paths is shifted, and input values to the scan paths for three bits are inverted. In concrete, in the fourth pattern, a random pattern shifting operation of inverting only a value of the scan path #1 ("0" being inverted to "1") is carried out. In the fifth pattern, only a value of the leading F/F of the scan path #4 is inverted ("1" being inverted to "0"). In the sixth pattern, only a value of the leading F/F of the scan path #127 is inverted ("1" being inverted to "0"). In the fifth pattern and the sixth pattern, the shift clock is not supplied to the LFSR 2 and F/Fs on the scan paths excepting the leading F/Fs. In the seventh pattern where all the bits are "0," the random pattern shifting operation is carried out.

[0046]

Values of the F/Fs on the scan paths at the time that the above seven patterns are applied from the tester are shown in FIG. 6. FIG. 6 is a diagram for illustrating

a result of the shift of the input pattern example. In FIG. 6, "-" represents an F/F to which a random pattern from the LFSR is set, whereas "F" represents an F/F to which a value of the random pattern which has been inverted is set since a value of the random pattern of the LFSR 2 differs from a value required by the ATPG.

[0047]

In the above manner, values required by the ATPG can be set to the internal F/Fs. Namely, when pure random pattern shifting and inverting of only one bit are carried out, the shifting of one stage is completed with one pattern. However, when not less than two bits are inverted, patterns equal in number to inverted bits are required for the shifting of one stage. From the fact shown in FIG. 2, an increase in the number of patterns caused by that multiple bits are inverted hardly occurs, but multiple scan paths allow improvement of the degree of parallelizing so that the testing time can be shortened. Additionally, the amount of data to be stored in the tester can be decreased according to the degree of parallelizing.

[0048]

FIG. 7 is a diagram illustrating an output verifying part according to the embodiment of this invention. In this example, it is assumed that the MISR 7 is used as the output verifier, and the number of the scan paths is 128. The output verifying part comprises the MISR 7 and the space compactor 6, where outputs from the 128 scan

paths #0, #1, ..., and #127 are compressed to about the number of bits of the MISR 7 by the space compactor 6, and the compressed data is further compressed by the MISR 7 and stored. To the mask 5, the control signals are inputted through the eight control input pins (b1 to b8). Additionally, outputs of the last F/Fs and outputs of F/Fs that are the last but one on the 128 scan paths #0, #1, ..., and #127 are inputted to the mask 5. Outputs of the 128 scan paths are connected to the input side of the last F/Fs on the scan paths, respectively. The mask 5 controls a shift clock to the MISR 7 (and to LFSR 2) and a shift clock to the F/Fs on the scan paths. When the indeterminate state is masked, only the shift clock for the last F/Fs on the scan paths #0, #1, ..., and #127 is applied, whereas the shift clock for other F/Fs on the scan paths and the MISR 7 (and LFSR 2) is suppressed.

[0049]

The mask 5 enables the masking operation at the highest bit (b1) of the control input, and has the decoder circuit 31 to which lower seven bits of the control input are inputted. An indeterminate value (X state value) inputted to a specific one of the 128 scan paths is masked and converted to a "1" state value (or a "0" state value) by the OR circuit (or the AND circuit).

[0050]

Namely, when "1" is inputted to the control input pin b1, and output of the OR circuit 36 becomes "1."

Accordingly, the shift clock (negative clock) to F/Fs other than the last F/Fs on the scan paths and the MISR 7 (and the LFSR 2) is suppressed, and the multiplier 33 feeds back the output of the last F/F according to "1" of the control input pin b1, and outputs it to the OR circuit 32. For this, "1" is outputted from the decoder circuit 31, whereby the indeterminate value (X state value) inputted to a specific one of the 128 scan paths can be masked and converted to the "1" state value by the OR circuit 32. When there is also the indeterminate value in an F/F on another scan path at the same time, the indeterminate value from the F/F is masked at the next shift clock.

[0051]

Although the pattern generating part and the output verifying part are basically independent, it is possible to share the lower seven bits of the control input when the circuits are both applied.

[0052]

As described above in the embodiment, a deterministic test pattern generated by the ATPG can be applied to an integrated circuit (LSI) within a short time. In concrete, by increasing the number of the internal scan paths by n times, it is possible to shorten the testing time to about 1/n.

[0053]

Concurrently, it is possible to decrease the amount of data to be stored in the tester. In concrete,

by increasing the number of the internal scan paths by n times, it is possible to decrease the memory quantity to 1/n.

[0054]

Although a pattern generator (LFSR 2 or the like) used in BIST is made use in this invention, such severe design limitations that a specific control circuit for the bus circuit is inserted, a circuit at a test point is inserted for improvement of the detection ratio and so forth are not placed on the designer since a deterministic pattern is applied to the inside. A pattern compactor (MISR 7 or the like) used in BIST can be used. Use of the mask 5 can prevent propagation of the indeterminate state inside the circuit to the MISR 7, which can avoid occurrence of a situation that the verification becomes impossible.

[0055]

Further, the above integrated circuit (LSI), the LFSR 2, the phase shifter 3, the pattern modifier 4, the scan paths #0, #1, …, and #n-1, the mask 5, the space compactor 6, the MISR 7 and so force can be simulated on the computer, and the test data can be created before the actual integrated circuit is manufactured.

[0056]

[Effects of the Invention]

As describe above, the present invention provides the following effects.

[0057]

(1) Since test patterns generated by the pattern generator built in the integrated circuit are modified by the pattern modifier, and inputted to a plurality of shift registers, the number of scan paths that are the shift registers is increased, thus the number of stages of the scan path can be decreased. This allows the time of a test on the integrated circuit (LSI) to be largely shortened. At this time, only significant data (information on F/Fs which need to be set values) is supplied from a tester (external input) and modified, so that the amount of data to be stored in the tester is largely decreased.

[0058]

(2) The indeterminate state in outputs from the plural shift registers configured with the sequential circuit elements inside the integrated circuit is masked, and a masked output result is verified by the output verifier. Whereby, the indeterminate state (X state) does not spoil a result of compression even if the results from the F/Fs are compressed and read out to the outside.

[0059]

(3) Test patterns generated by the pattern generator built in the integrated circuit are modified by the pattern modifier and inputted to the plural shift registers, the indeterminate state in outputs from the plural shift registers is masked and converted to the specified state, and the masked output result is verified by the output verifier. It is thereby possible to increase

the number of the scan paths to shorten the time period of the test on the integrated circuit. It is also possible to decrease the amount of data to be stored in the tester because only meaningful data is supplied from the tester (external input) and modified, and to prevent a result of the compression from being spoiled by the indeterminate state even if results of the internal FFs are compressed and read out to the outside.

[0060]

(4) The output verifier has a means for compressing the masked output result so that the results of the internal FFs can be efficiently stored in the output verifier.

[Brief Description of the Drawings]

[FIG. 1] Diagram for illustrating a principle of this invention;

[FIG. 2] Diagram for illustrating a state of distribution of the number of set F/Fs in ATPG according to an embodiment;

[FIG. 3] Diagram showing a testing apparatus according to the embodiment;

[FIG. 4] Diagram showing a pattern generating part according to the embodiment;

[FIG. 5] Diagram for illustrating setting of random numbers and ATPG according to the embodiment;

[FIG. 6] Diagram for illustrating shift results of examples of input patterns according to the embodiment

[FIG. 7] Diagram showing an output verifying part according

to the embodiment;

[FIG. 8] Diagram for illustrating a known scan design; and

[FIG. 9] Diagram for illustrating a known BIST circuit.

[Explanations of Letters or Numerals]

2a … pattern generator

4 … pattern modifier

5 … mask

7a … output verifier

#0-#n-1 … shift register (scan path)

[Name of Document] ABSTRACT

[Abstract]

[Object]

To Enable a high-quality test within a short period of time, and dispense with an expensive tester without placing severe design limitations on the designer.

[Means for Solution]

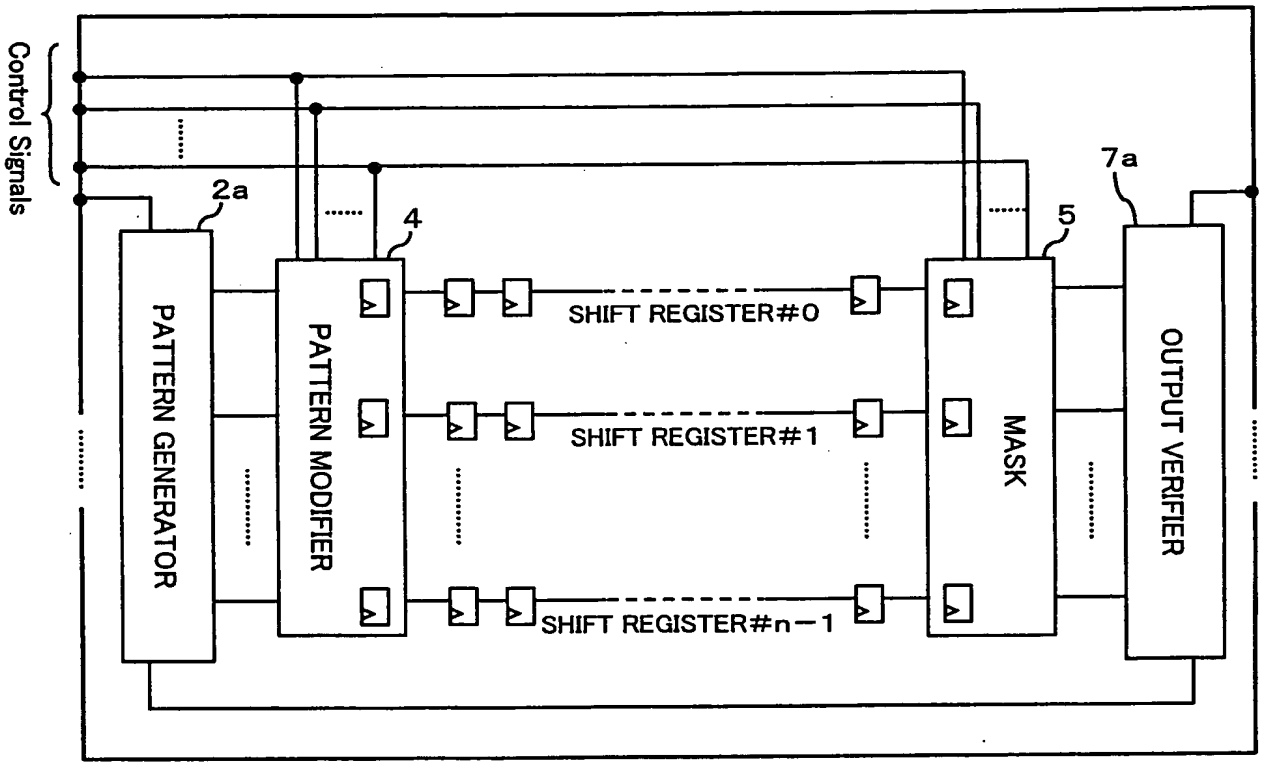
An apparatus comprises a pattern generator 2a built in an integrated circuit to generate test patterns, a pattern modifier 4 modifying the generated test patterns according to external inputs, and a plurality of shift registers #0 to #n-1 configured with sequential circuit elements inside the integrated circuit, wherein the test patterns modified by the pattern modifier 4 are inputted to the plural shift registers #0 to #n-1.

[Chosen Drawing] FIG. 1

[NAME OF THE DOCUMENT] Drawings

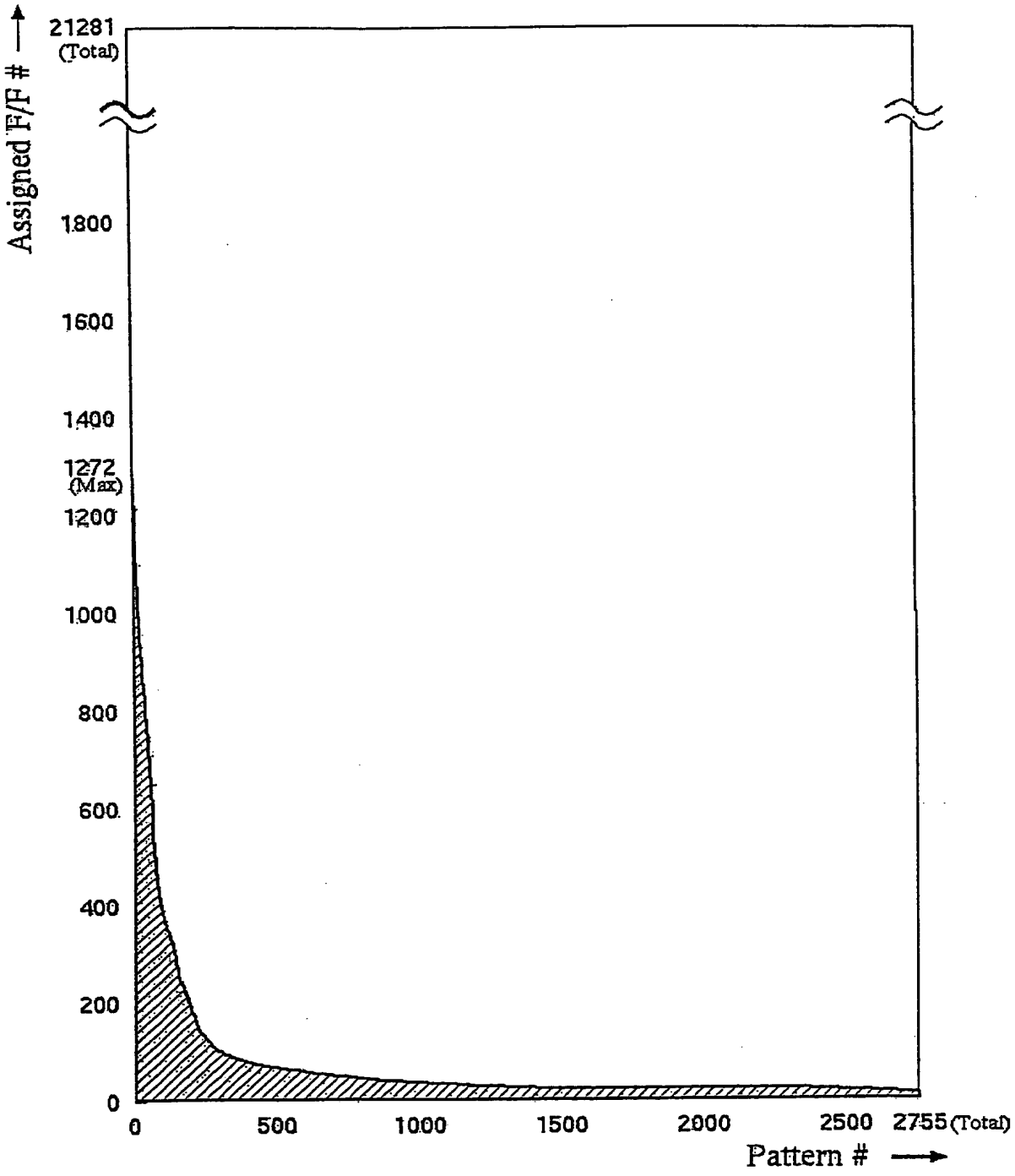
[FIG.1]

Diagram for illustrating a principle of this invention



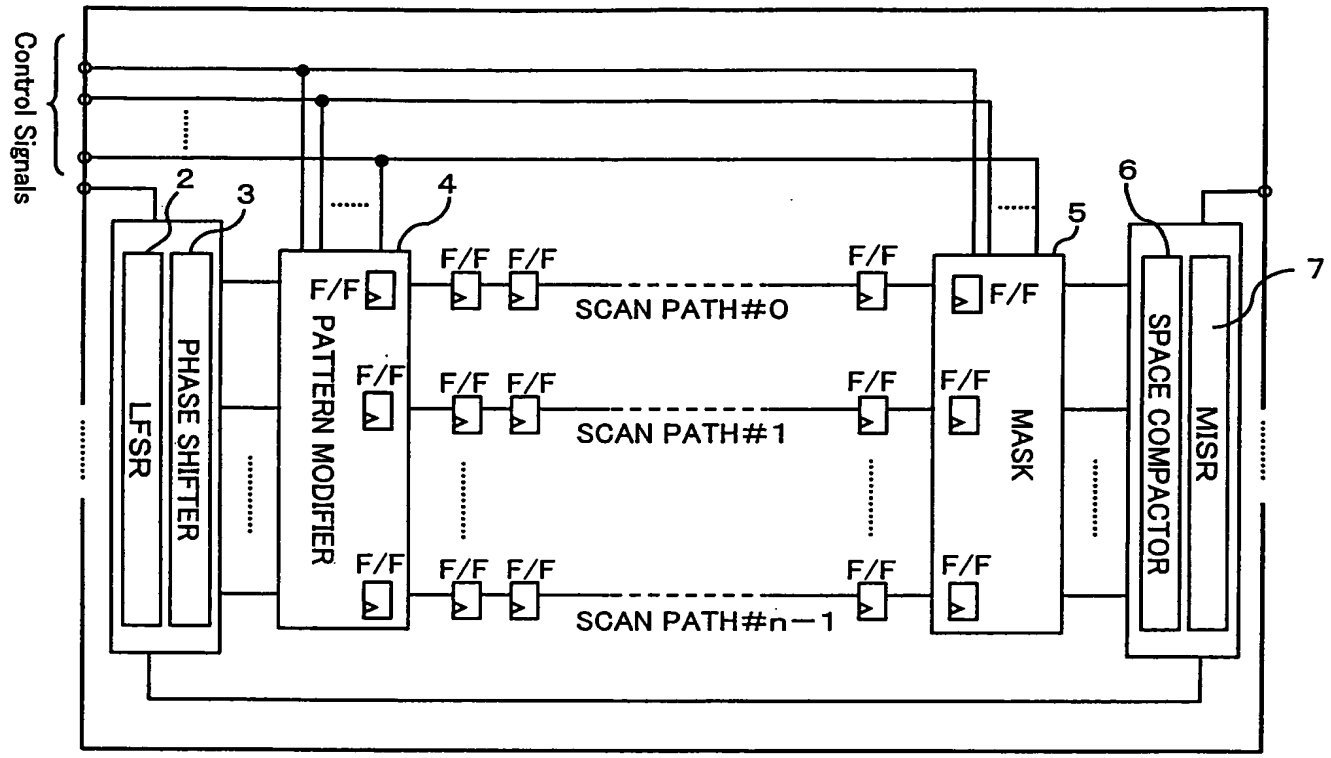
[FIG.2]

Diagram for illustrating a state of distribution of the number of set F/Fs in ATPG



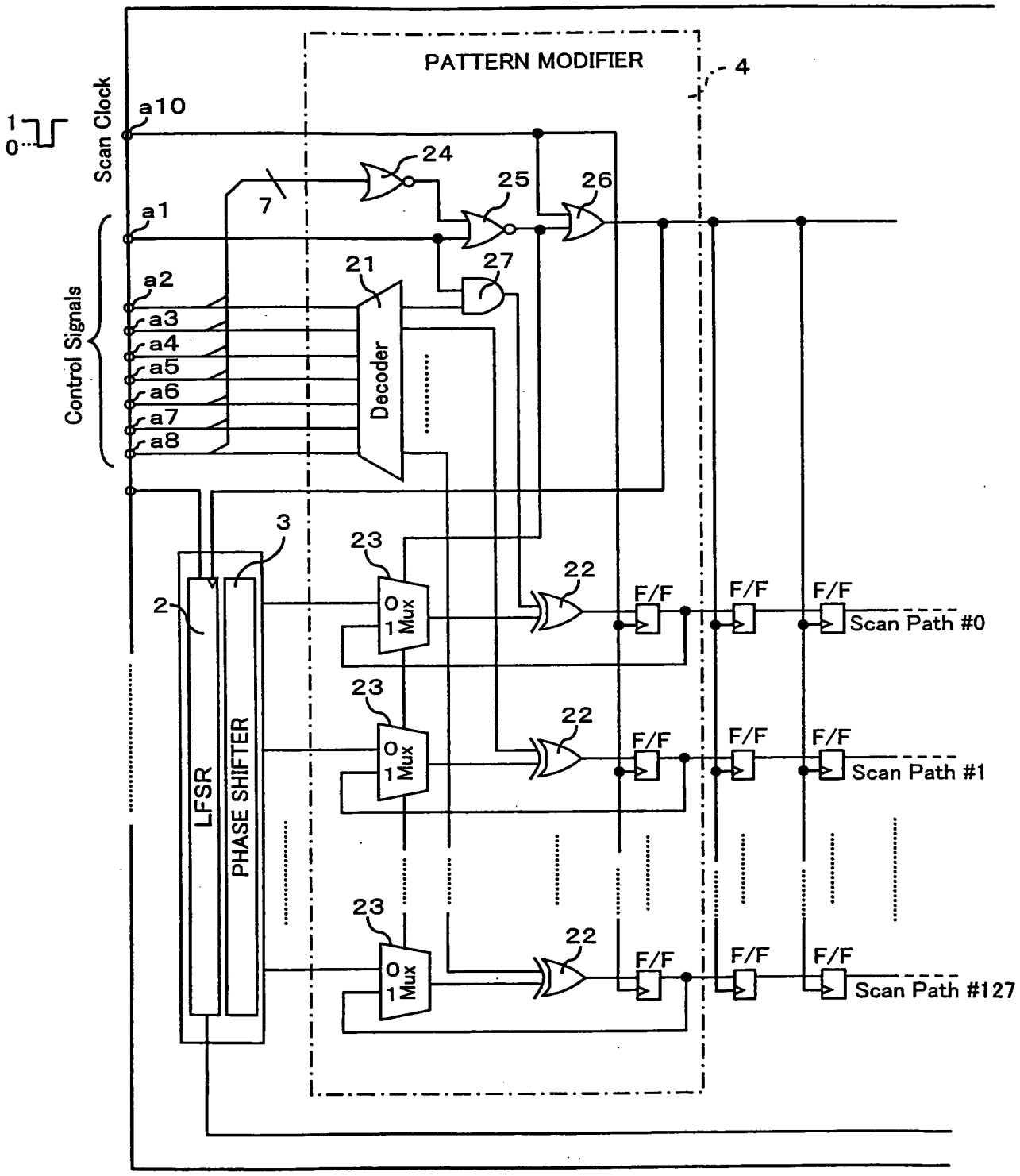
[FIG.3]

Diagram showing a testing apparatus



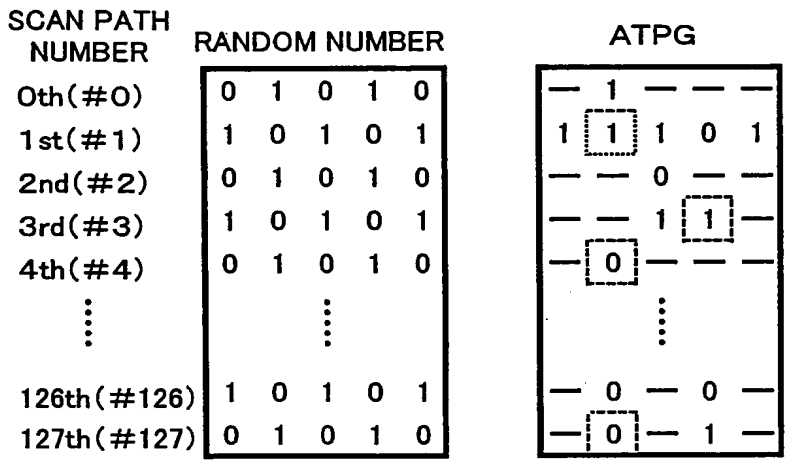
[FIG.4]

Diagram showing a pattern generating part

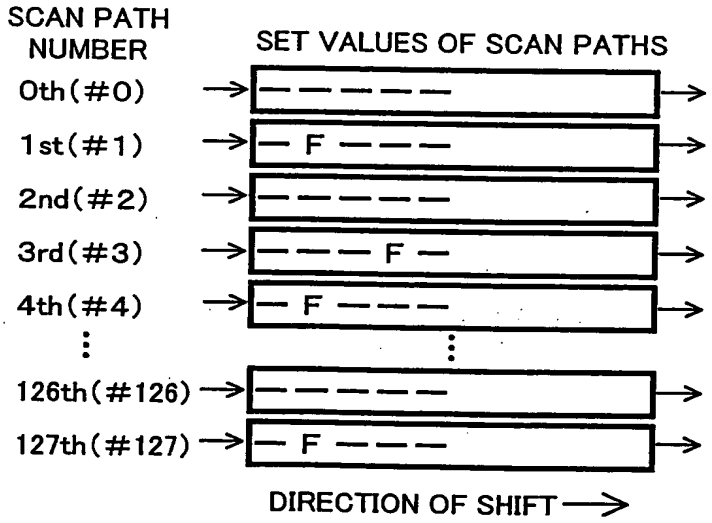


[FIG.5]

Diagram for illustrating setting of random numbers and ATPG

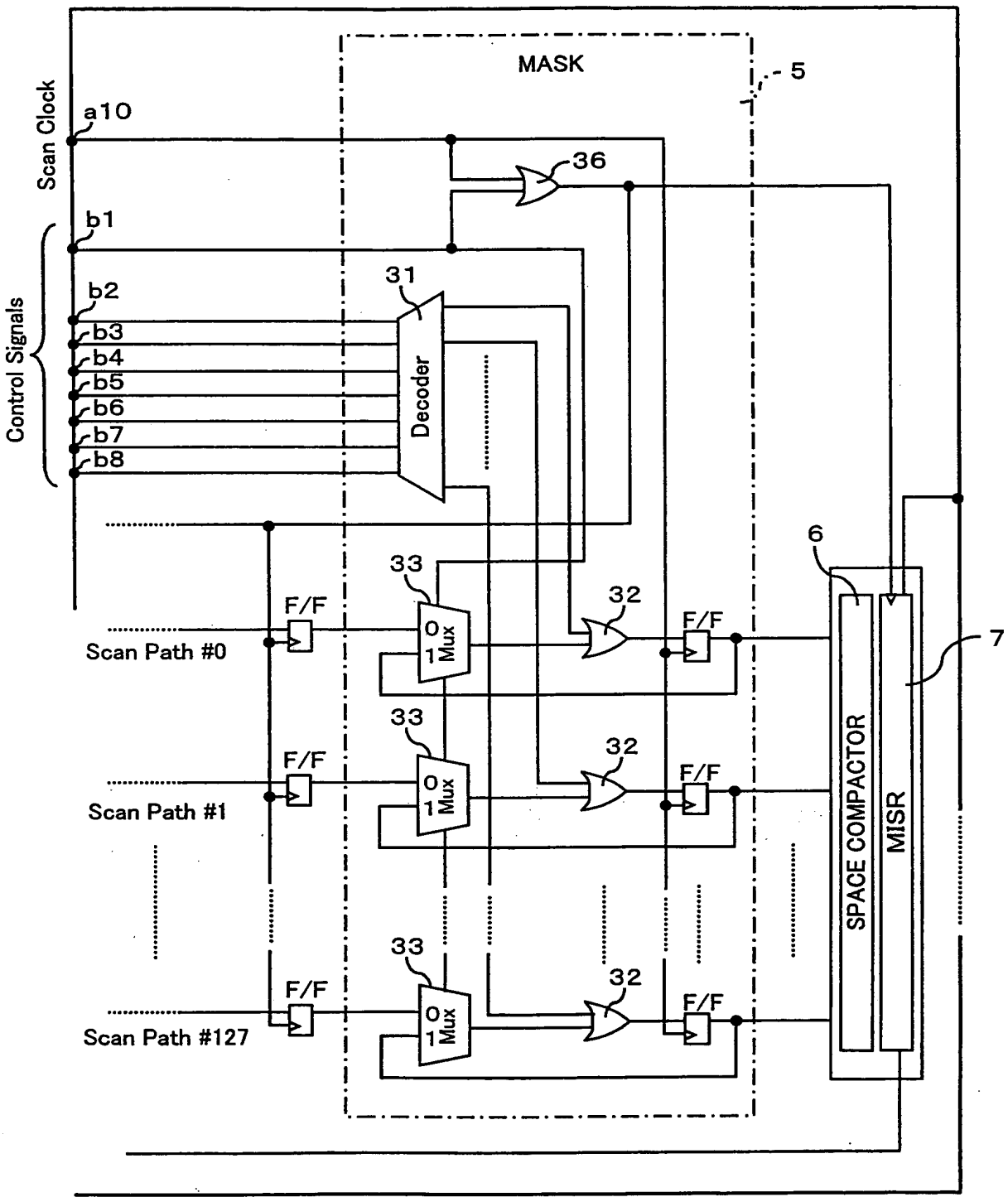


[FIG.6] Diagram for illustrating shift results of examples of input patterns



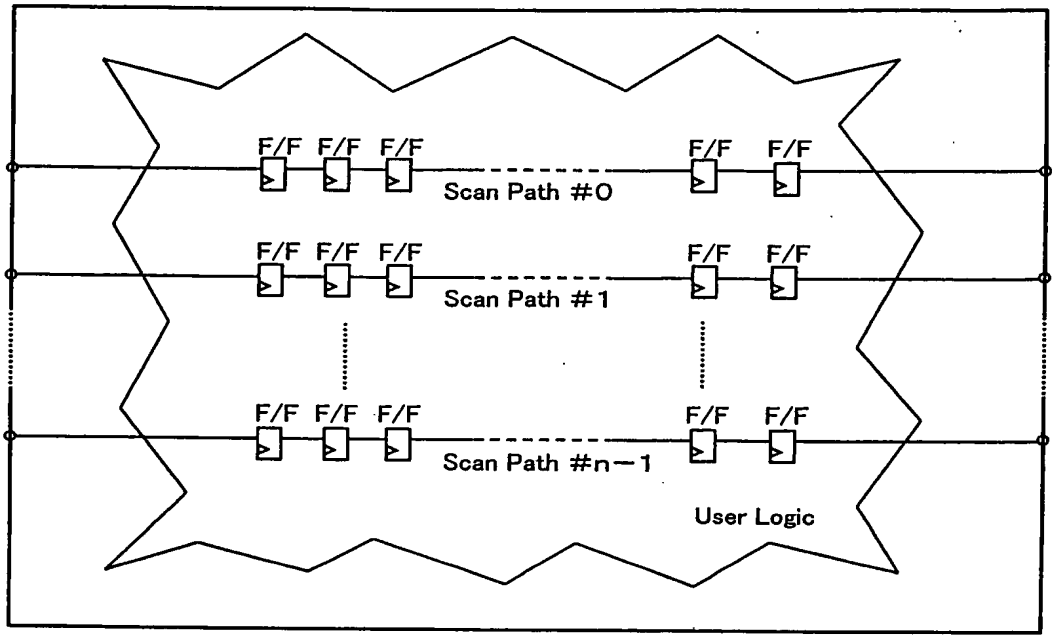
[FIG.7]

Diagram showing an output verifying part



[FIG.8]

Diagram for illustrating a known scan design



[FIG.9]

Diagram for illustrating a known BIST circuit